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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,793	09/08/2003	James M. Norris	CML00107D P01	1369

33117 7590 12/05/2005

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EXAMINER	
KIM, HONG CHONG	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 12/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/657,793	NORRIS ET AL.	
	Examiner	Art Unit	
	Hong C. Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1-9 and 11-24* is/are rejected.

7)☒ Claim(s) *10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/8/03 6/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. Claims 1-25 are presented for examination. This office action is in response to the application filed on 9/8/2003.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 9/8/2003 and 06/01/2005 are being considered by the examiner.

3. The drawings are objected to under 37 C.F.R. § 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "first, second and third counters" must be shown or the feature cancelled from the claim. No new matter should be entered.

4. The U.S. applications referred to by Attorney Docket Numbers in the specification (i.e .page 1) should be changed to the U.S. patent application serial numbers as appropriate. Also, the status of the referenced U.S. applications must be updated accordingly (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.) in the Related Applications section and in any other corresponding area in the specification, if any.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The title should be more specific to differentiate the invention from similar inventions in the patent literature. "calculating address" "stride", "skip", "span", "type", and "first, second and third counters" aspects of the invention should be mentioned in the title so that the title is more descriptive.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-9, 11-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Scales, III et al. (Scales) US Patent No. 6,202,130.

As to claim 1, Scales discloses the invention as claimed. Scales discloses a system for addressing a vector of elements in a memory having a plurality of partitions (Fig. 1), the system comprising: a first storage element for storing a STRIDE value (Fig. 2 Ref. 108) denoting the separation between elements of the vector of elements within each partition of the plurality of partitions; a second storage element for storing a SKIP value (Fig. 2 refs. 108 and 116) related to the separation between the last element of the vector of elements in one partition of the plurality of partitions and the first element of the vector of elements in the next partition of the plurality of partitions; a third

storage element for storing a SPAN value (Fig. 2 Ref. 106) denoting the number of elements the vector of elements within each partition of the plurality of partitions; and an arithmetic unit (Fig. 3 ref. 302) coupled to the first, second and third storage elements and operable to calculate the address in the memory of a next element of the vector of elements dependent upon the values stored in the first, second and third storage elements and the address of a current element.

As to claim 2, Scales discloses the invention as claimed the above. Scales further discloses wherein the STRIDE and SKIP values denote a number of elements and further comprising: a fourth storage element for storing a TYPE value (Fig. 2 Ref. 104) denoting the size of each element of the vector of elements; wherein the arithmetic unit is coupled to the fourth storage element and is operable to calculate the address in the memory of a next element (Fig. 3 ref. 306) of the vector of elements dependent upon the values stored in the first, second, third and fourth storage elements and the address of a current element.

As to claim 3, Scales discloses the invention as claimed the above. Scales further discloses wherein operation of the arithmetic unit is dependent upon an initial element address EA_START 9Fig. 2 Ref. 112) that is indicative of the address of the first element in the vector of elements.

As to claim 4, Scales discloses the invention as claimed the above. Scales further discloses wherein operation of the arithmetic unit is further dependent upon the number of elements LEFT_START (Fig. 1 Ref. 114) in the first partition of the plurality of partitions.

As to claim 5, Scales discloses the invention as claimed the above. Scales further discloses wherein the system is operable to address a specified number of elements (Fig. 2).

As to claim 6, Scales discloses the invention as claimed the above. Scales further discloses wherein the arithmetic unit is operable to receive a control instruction indicative of the TYPE, STRIDE, SKIP and SPAN values (Figs. 2 and 3).

As to claim 7, Scales discloses the invention as claimed the above. Scales further discloses wherein the arithmetic unit is operable to receive a control instruction indicative of the address of the first element EA_START (Fig. 2 ref. 112), the number of elements LEFT_START (Fig. 2 ref. 114) in the first partition of the plurality of partitions and the total number of elements TOTAL (Fig. 2 ref. 104) to be addressed.

As to claim 8, Scales discloses the invention as claimed the above. Scales further discloses wherein the arithmetic unit includes: a first counter for counting a

LEFT value (Fig. 2 ref. 104) indicative of the number of elements remaining in a current memory partition; a second counter for counting a COUNT value indicative of the total number of elements still to be accessed (Fig. 2 Ref. 106).

As to claim 9, Scales discloses the invention as claimed the above. Scales further discloses wherein the arithmetic unit is operable to reset the first counter when the end of a partition is reached (col. 7 line 21).

As to claim 11, Scales discloses the invention as claimed. Scales discloses a processing system operable to access a partitioned memory (Fig. 1), the processing system comprising: a processing unit (Fig. 1) having a plurality of functional elements; an external interface; an input unit coupled to the processing unit and the external interface and operable to retrieve a vector of elements from the memory via the external interface and pass them to the processing unit, the input unit having a set of input storage elements for storing STRIDE, SKIP and SPAN values (fig. 2) and an input arithmetic unit operable to calculate the address in the memory of a next element of the vector of elements dependent upon the STRIDE, SKIP and SPAN values and the address of a current element; an output unit coupled to the processing unit and the external interface and operable to retrieve a result value from the processing unit and pass it to the external interface; and a program sequencer (fig. 1 ref. 17) coupled to and operable to control the processing unit, the input unit and the output unit.

As to claim 12, Scales discloses the invention as claimed the above. Scales further discloses wherein the input unit has an additional input storage element for storing a TYPE value (fig. 1 ref. 104) and wherein the input arithmetic unit is operable to calculate the address in the memory of a next element of the vector of elements dependent upon the TYPE, STRIDE, SKIP and SPAN values and the address of a current element

As to claim 13, Scales discloses the invention as claimed the above. Scales further discloses wherein the output unit is operable to store a vector of elements received from the processing unit to the memory via the external interface, the output unit having a set of output storage elements to store TYPE, STRIDE, SKIP and SPAN values and an output arithmetic unit operable to calculate the address in the memory of a next element (fig. 3 Ref. 306) of the vector of elements dependent upon the TYPE, STRIDE, SKIP and SPAN values and the address of a current element.

As to claim 14, Scales discloses the invention as claimed the above. Scales further discloses wherein the external interface is a memory interface and further comprising a memory unit (Fig. 1 ref. 14 or 16) coupled to the memory interface.

As to claim 15, Scales discloses the invention as claimed. Scales discloses a

method for accessing a vector of elements in a memory having a plurality of partitions, comprising: accessing the memory at an element address in a partition; stepping a first counter (Fig. 2 ref. 108 and col. 5 lines 10+); and if a second counter (Fig. 2 ref. 106) indicates that at least one vector element remains in the partition: incrementing the element address by a first amount; and stepping the second counter; otherwise: incrementing the element address by a second amount; and resetting the second counter to indicate the number of elements of the vector of elements in a partition.

As to claim 16, Scales discloses the invention as claimed the above. Scales further discloses wherein the first amount is a product of the size of an element and the number of memory elements between adjacent vector elements in a partition (col. 5 lines 10+).

As to claim 17, Scales discloses the invention as claimed the above. Scales further discloses wherein the first amount is a difference between consecutive vector element addresses in a partition (col. 5 lines 10+).

As to claim 18, Scales discloses the invention as claimed the above. Scales further discloses wherein the second amount is a product of the size of an element and the number of elements between last element of one partition and the first element of the next partition (col. 5 lines 10+).

As to claim 19, Scales discloses the invention as claimed the above. Scales further discloses wherein the second amount is a difference between the last vector element address in one partition and the first vector element address in the next partition (col. 5 lines 10+).

As to claim 20, Scales discloses the invention as claimed the above. Scales further discloses wherein the element address is initialized as the address of the first element in a partition and wherein the first counter is initialized to indicate the number of elements of the vector of elements in the first partition of the plurality of partitions, thereby allowing memory access to begin part way through the first partition (col. 5 lines 10+ and col. 7 lines 12+).

As to claim 21, Scales discloses the invention as claimed the above. Scales further discloses wherein accessing the memory at the element address in a partition comprises reading a value of appropriate size stored at the element address (col. 5 lines 10+).

As to claim 22, Scales discloses the invention as claimed the above. Scales further discloses wherein accessing the memory at the element address in a partition comprises storing a value of appropriate size at the element address (col. 5 lines 10+).

As to claim 23, Scales discloses the invention as claimed the above. Scales further discloses wherein the first counter, the second counter and the element address are not re-initialized if the memory access is interrupted and resumed before all of the elements of the vector have been accessed (col. 5 lines 10+ and col. 7 lines 12+).

As to claim 24, Scales discloses the invention as claimed the above. Scales further discloses wherein the first amount and the second amount are set to default values unless otherwise specified (col. 5 lines 10+ and col. 7 lines 12+).

Allowable Subject Matter

7. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. Claim 25 is allowed.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See attached PTO-892.

2. A shortened statutory period for response to this action is set to expire 3 (three)

months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

3. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

4. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong Kim whose telephone number is (571) 272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 whose telephone number is (571) 272-2100.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

7. **Any response to this action should be mailed to:**

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to TC-2100:
(571)-273-8300

Hand-delivered responses should be brought to the Customer Service Window (Randolph Building, 401 Dulany Street, Alexandria, VA 22314).

H Kim
Primary Patent Examiner
November 29, 2005